

REMARKS

Claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47, as amended, are before the Examiner for consideration. Claims 3-11, 13-15, 17-19, 21-23, 25-30, 32-34, 36-38, 40-42, 44-46 and 48-50 are pending but stand withdrawn from consideration as directed to non-elected inventions.

Claim 1 has been amended to recite an error-detecting data transfer sub means for transferring error-corrected data from said buffer memory to said error detecting means in code word units for error detection, after said error correcting means corrects an error contained in data in said buffer memory based on the syndrome transmitted by said syndrome calculating means, said transferred error-corrected data including a code word from which the error-containing data has been detected up to and a final code word; and also to recite an after-correction error detecting sub means for executing error detection after said syndrome calculating means detects an error-containing data, for data transferred from said buffer memory after an error correction done by said error correcting means, following a code word at which an error code is detected using mid-term results

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already stored in said storing means, of code words before detection of an error code. See applicants' Figs. 4, 6, 8, 10 and 11 which support this claimed feature.

The specification has been edited to remove references to the claims.

1. The finality of the restriction requirement is acknowledged. Applicants will rely upon the protections afforded by 35 USC §121 regarding any divisional application.

2. The drawings were objected to for expressly stated reasons. Submitted herewith are copies of duplicate Figures 4, 6, 8, 10 revised to include reference characters "a-1" to "a-12" (and similarly for "b," "c" and "d"), and Figure 11 revised to include reference characters 5, 7, 9a and 10a. Withdrawal of the objection to the drawings is respectfully requested.

3. The Abstract has been revised. The stated objection has been overcome.

4. Claim 1 was objected to for specific reasons. Each informality has been addressed, thereby mooting those objections.

5. Claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47 were rejected under 35 U.S.C. §112, second paragraph for reasons given on pages 22-26 of the Office Action. Claim 1 has been amended to moot the rejection. Antecedent basis in claim 1 is now clear; the claim is believed to be definite. Reconsideration and withdrawal of the rejection are respectfully requested.

6. Claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47 were rejected under 35 U.S.C. §103(a) as unpatentable over Zook U.S. Patent 5,592,498 in view of Zook U.S. Patent 5,991,911. The rejection is respectfully traversed.

The presently claimed error correction device includes an error detecting means including (1) a parallel process sub means and (2) an after-correction error detecting sub means for executing error detection after the syndrome calculating means

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detects an error-containing data, for data transferred from the buffer memory after an error correction done by the error correcting means, following a code word at which an error code is detected using mid-term results already stored in said storing means, of code words before detection of an error code. This arrangement is nowhere disclosed in or suggested by the cited references.

Zook '498 describes error detection performed in detection circuit CHECKER 70 in parallel with syndrome calculation. If there is an error in data (GDAT), an error pattern (ERR) calculated in CORRECTOR 60 is inputted into CHECKER 70, and the mid-term result of error detection calculated with respect to uncorrected data is amended. Thus, rather than start the error detection calculation again, the mid-term result of error detection is amended and error detection then proceeds. In Zook '498, to amend the mid-term result of error detection calculated using uncorrected data, the error detection circuit needs, for example, a multiplier 716 for byte synchronization and adder 706.

The presently claimed invention has the same purpose as the system of Zook '498, i.e., to increase the rate of processing by performing error detection in parallel with the syndrome calculation. However, the presently claimed invention patentably differs from Zook '498 in how to deal with erroneous data. In the presently claimed invention, the mid-term result of error detection calculation is stored in the storing means. When data has an error, the error detector reloads the last-stored detection calculation result, and error detection calculation resumes using correct data in which the error has been corrected. Because the last-stored detection calculation result is one calculated using correct data, there is no need to amend, using an error pattern, the mid-term result of error detection calculated using uncorrected data, as required by Zook '498. The presently claimed invention has the unique advantageous effect of increasing the rate of processing with a simple structure, as compared to either Zook '498 or Zook '911. Neither Zook '498 or Zook '911 disclose or suggest an after-correction error detecting sub means for executing error detection after the syndrome calculating means detects an error-

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containing data, for data transferred from the buffer memory after an error correction done by the error correcting means, following a code word at which an error code is detected using mid-term results already stored in said storing means, of code words before detection of an error code, as recited in applicants' claim 1.

Zook '911 is cited for its teaching of a product code including inner and outer parity. But Zook '911 does not overcome the deficiencies of Zook '498 explained herein.

Claims 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47, which depend from claim 1, are allowable for the same reasons that claim 1 is allowable. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

All claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47 are now proper in form and patentably distinguished over all grounds of rejection stated in the Office Action. Accordingly, allowance of all claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47 is respectfully requested.

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The Examiner's comment that no certified copy of the priority document has been received is acknowledged. No claim for priority under 35 USC §119 has been made in this case.

The Examiner is thanked for listing the references submitted with an Information Disclosure Statement.

Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicants' undersigned representatives. If the only barrier to allowance is the presence of the non-elected claims, the Examiner is authorized to cancel those claims for that express purpose.

Respectfully submitted,

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IN THE DRAWINGS:

Please enter the attached five (5) sheets of formal drawings, Figures 4, 6, 8, 10 and 11, to replace Figures 4, 6, 8, 10 and 11 as originally filed.



Fig. 4

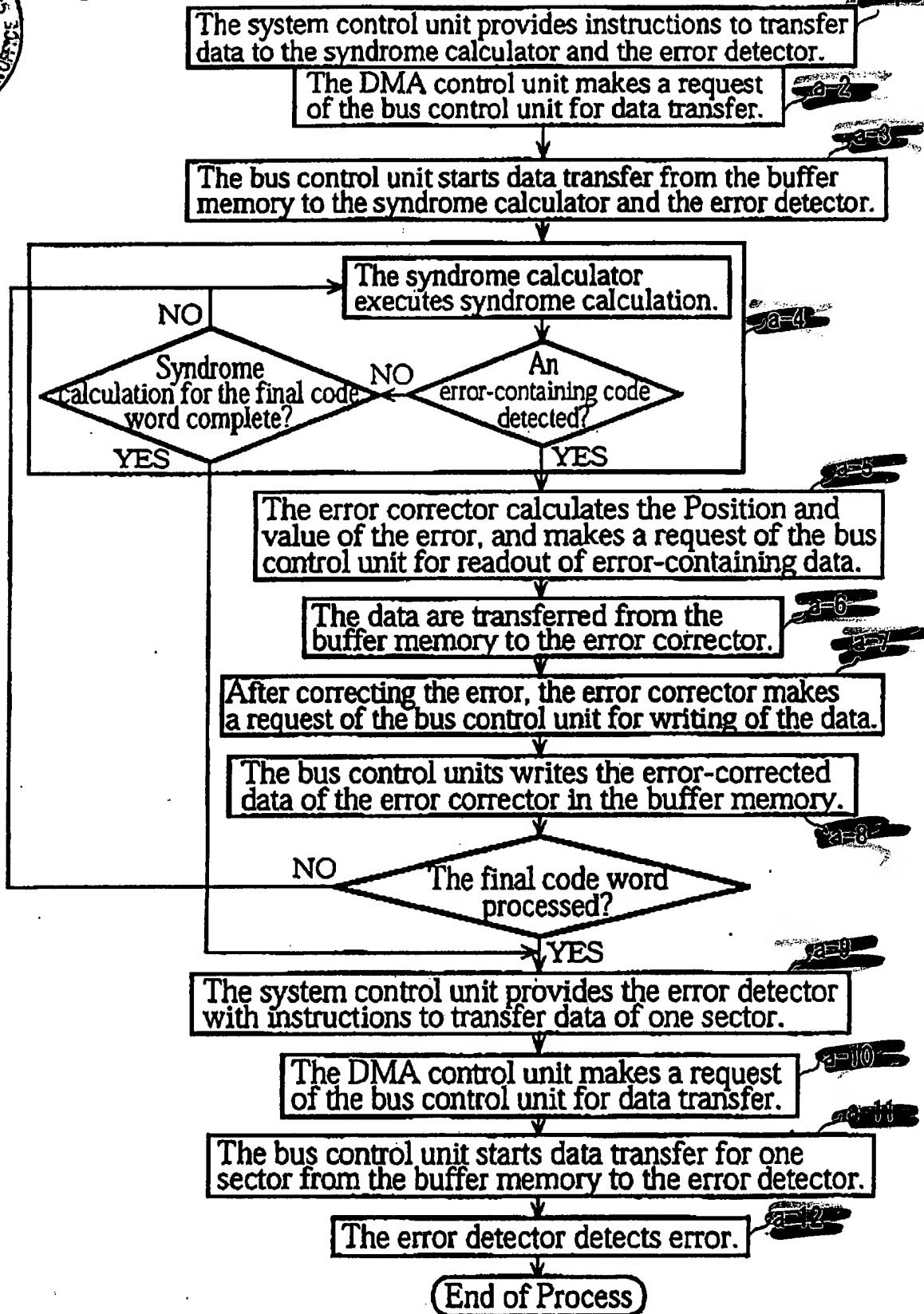




Fig. 6

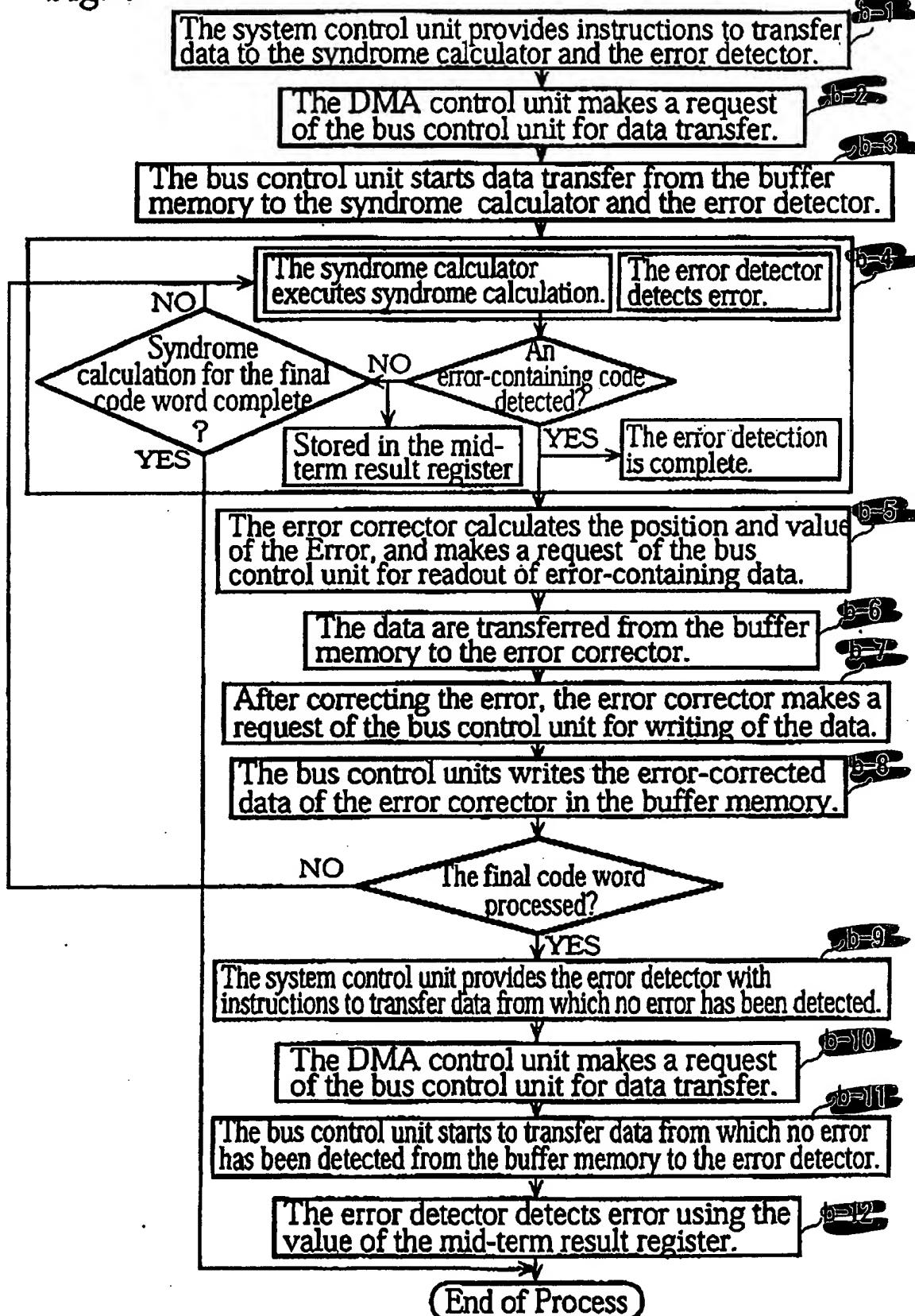
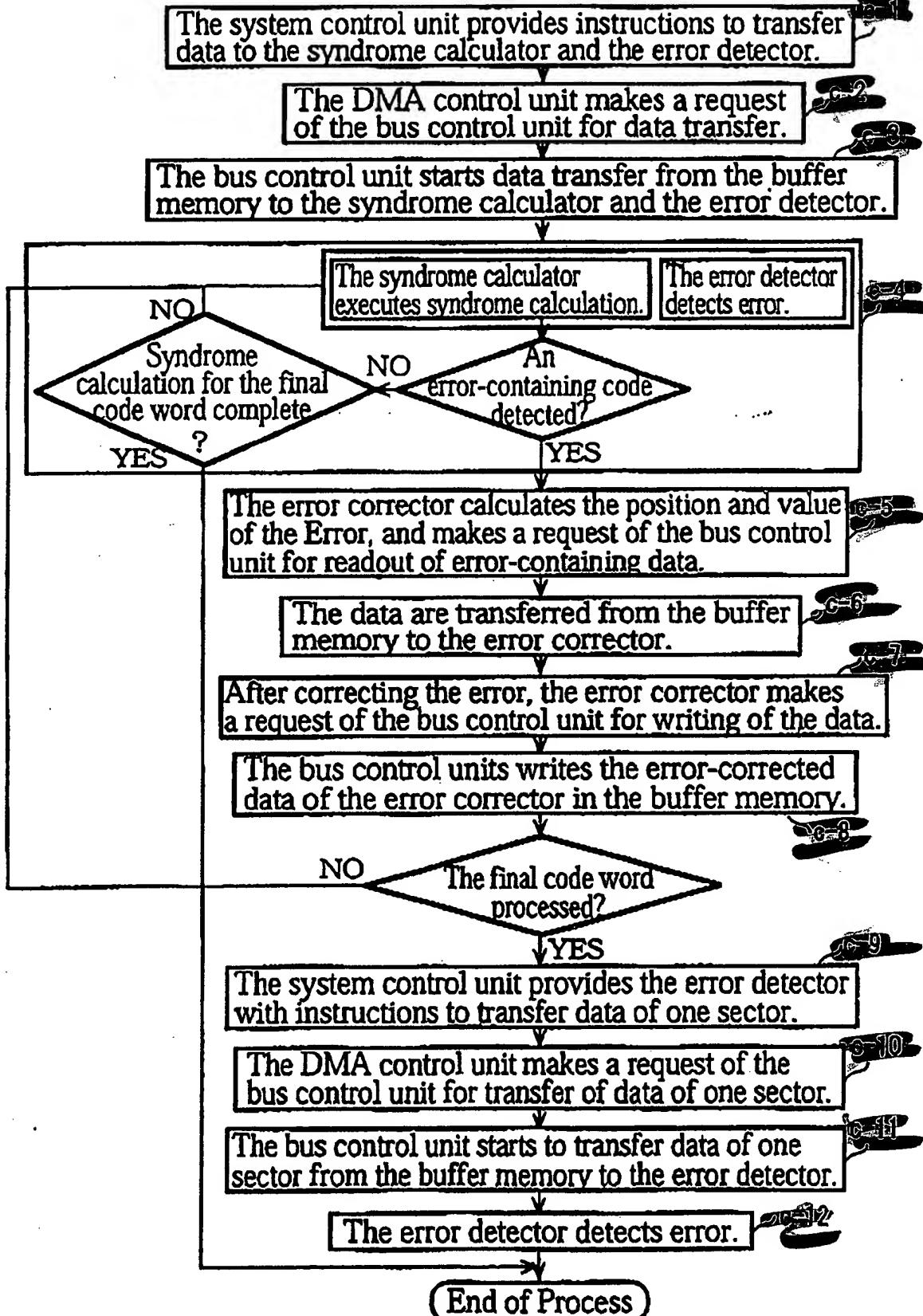




Fig. 8



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Fig. 10

The system control unit provides instructions to transfer data to the syndrome calculator and the error detector.

The DMA control unit makes a request of the bus control unit for data transfer.

The bus control unit starts data transfer from the buffer memory to the syndrome calculator and the error detector.

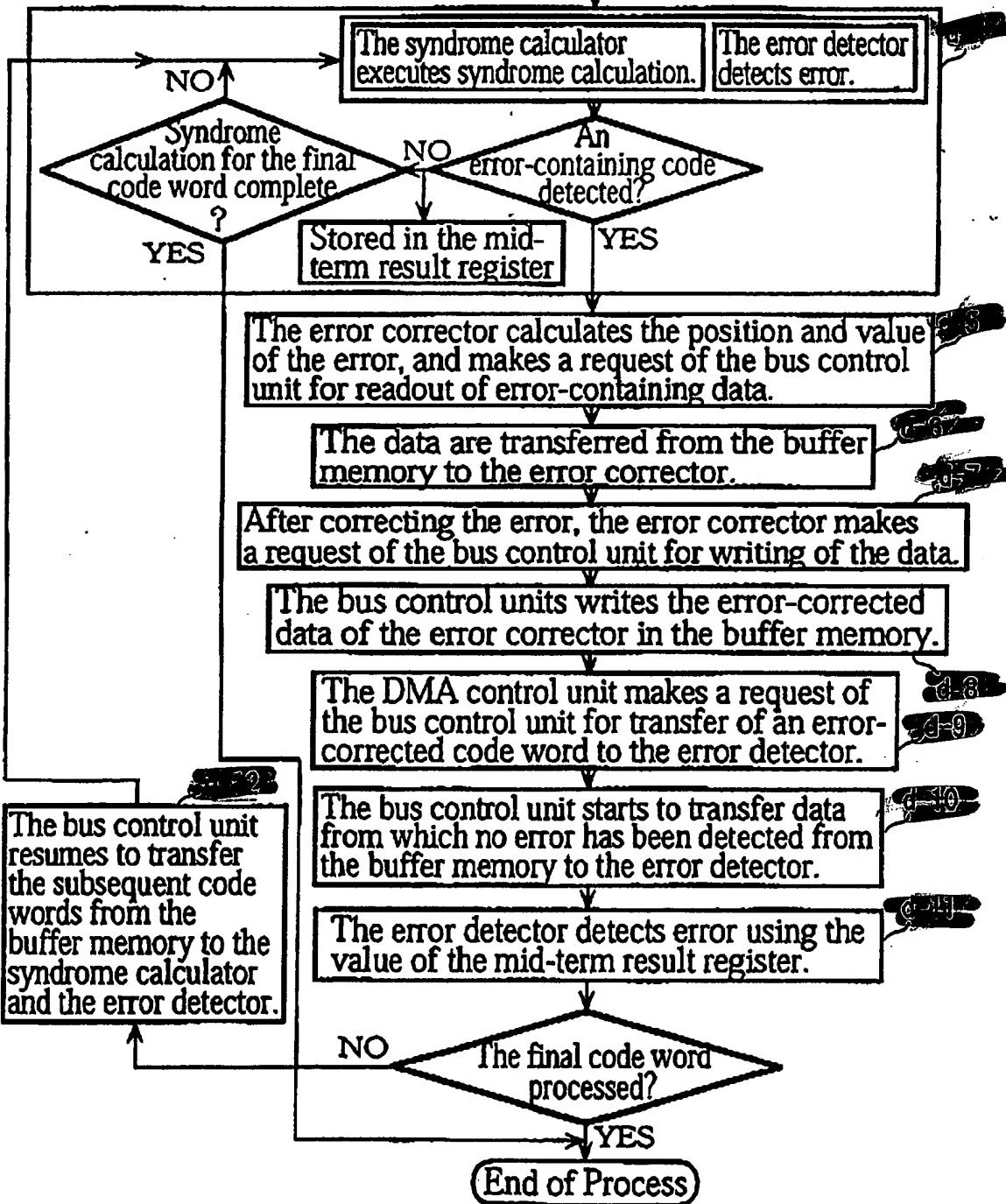




Fig. 11

